

High Speed Serdes Devices And Applications

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High Speed Serdes Devices and Applications provides a broad understanding of High Speed Serdes (HSS) device usage. The material focuses on HSS devices, and the consolidation of related topics into a single text.

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as has silicon density, and this has led to a prevalence of High Speed Serdes (HSS) devices as an inherent part of almost any chip design. HSS devices are the dominant form of input/output for many (if not most) high-integration chips, moving serial data between chips at speeds up to 10 Gbps and beyond.

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Chip and system designers using HSS devices must have detailed knowledge of both the features and functions of the HSS device, and the applications in which they are used.

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A Serializer/Deserializer (SerDes pronounced sir-deez or sir-dez) is a pair of functional blocks commonly used in high speed communications to compensate for limited input/output. These blocks convert data between serial data and parallel interfaces in each direction. The term "SerDes" generically refers to interfaces used in various technologies and applications.

SerDes - Wikipedia

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When most system designers look at serializer/deserializer (SerDes) devices, they often compare speed and power without considering how the SerDes works and what it actually does with their data. Internal SerDes architecture may seem irrelevant, but this overlooked item can dictate many important system parameters like system topology,

SerDes Architectures and Applications (PDF)

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The use of twisted pair cabling is possible for high-speed serial data rates. Lattice SERDES devices allow easy system design migration into wired back-bone configurations. The use of SSP and UTP cables for patch-cord and cross connect jumpers is possible when the designer understands the attenuation trade-offs. To ensure overall sys-

TN1066 - Transmission of High-Speed Serial Signals Over ...

HSS devices are the dominant form of input/output for many (if not most) high-integration chips, moving serial data between chips at speeds up to 10 Gbps and beyond. Chip designers with a background in digital logic design tend to view HSS devices as simply complex digital input/output cells.

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